

What is claimed is:

1 1. In a thin film transistor having a back channel
 2 electrode, wherein a voltage of a front channel positioned
 3 on the side of a gate wiring of said thin film transistor
 4 is made equal to a voltage of said back channel positioned
 5 on the side of a back channel electrode by short-circuiting
 6 said back channel electrode to a gate electrode through a
 7 contact-hole provided in a portion of a semiconductor layer
 8 constituting said thin film transistor.

1 2. A thin film transistor as claimed in claim 1, wherein
 2 said back channel electrode is formed of the same material
 3 as a material of a pixel electrode connected to one of
 4 source and drain electrodes of said thin film transistor.

1 3. A thin film transistor as claimed in claim 2, wherein
 2 said pixel electrode is a transparent electrode.

1 ~~4. A thin film transistor as claimed in claim 1, wherein~~
 2 ~~said contact-hole is formed in a location remote from an~~
 3 ~~active region of said thin film transistor by at least five~~
 4 ~~microns.~~

1 5. A thin film transistor as claimed in claim 1, wherein
 2 a passivation film patterned to have a width equal to that
 3 of said back channel electrode and said semiconductor layer

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4 are provided between said back channel and said gate
5 insulating film.

1 6. A thin film transistor as claimed in claim 1, wherein
2 said semiconductor layer patterned to have a width equal to
3 that of said source and drain electrodes of said thin film
4 transistor is provided between said source and drain
5 electrodes and said gate insulating film.

1 7. A thin film transistor as claimed in claim 1, wherein
2 said semiconductor layer has an ohmic contact layer on the
3 side thereof, which is in contact with said source and
4 drain electrodes.

1 8. In a fabrication method of a thin film transistor,
2 including the steps of forming a gate electrode wiring
3 pattern and a gate insulating film on a substrate and
4 forming a semiconductor layer and a source and drain
5 electrodes on said gate insulating film, forming a pixel
6 electrode connected to one of said source and drain
7 electrodes and forming a passivation film and a back
8 channel electrode on an active region of said thin film
9 transistor, said fabrication method comprising the steps of
10 patterning said source and drain electrodes without
11 patterning said semiconductor layer, forming said
12 passivation film after the patterning step, patterning a
13 gate contact hole for connecting said back channel

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14 electrode to said gate electrode and an opening portion for
15 said pixel electrode such that said gate contact hole and
16 said opening portion penetrate said passivation film, said
17 semiconductor layer and said gate insulating film, forming
18 an electrically conductive film for said pixel electrode
19 such that said conductive film commonly covers said gate
20 contact hole and said opening portion and patterning said
21 conductive film such that said pixel electrode and said
22 back channel electrode are left as they are, wherein said
23 passivation film and said semiconductor layer, which are
24 left as they are, are patterned simultaneously with using
25 said pixel electrode, said back channel electrode and said
26 source and drain electrodes, which are left as they are as
27 a mask.

1 9. A fabrication method as claimed in claim 8, wherein
2 said opening portion is provided by removing a portion of
3 the one of said source and drain electrodes, to which said
4 pixel electrode is connected.

1 10. A fabrication method as claimed in claim 8, wherein
2 said contact hole is formed in a location remote from said
3 active region of said thin film transistor.

1 11. A fabrication method as claimed in claim 8, wherein a
2 one side of said opening portion is formed such that one
3 side of one of said source and drain electrodes is exposed

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4 through said opening portion and is electrically connected
5 to said pixel electrode.

1 12. A fabrication method as claimed in claim 8, wherein
2 said semiconductor layer has an ohmic contact layer on the
3 side of said source and drain electrodes and said ohmic
4 contact layer on said active region is patterned
5 simultaneously with the patterning step of said source and
6 drain electrodes.

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